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09/751,601	12/29/2000	David I. Poisner	042390P9938	8581

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EXAMINER

SURYAWANSHI, SURESH

ART UNIT	PAPER NUMBER
2115	

DATE MAILED: 09/21/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/751,601

Applicant(s)

POISNER, DAVID I.

Examiner

Suresh K Suryawanshi

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 18 June 2004.
- 2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-16 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-16 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____

DETAILED ACTION

1. Claims 1-16 are presented for examination.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claim 1 is rejected under 35 U.S.C. 102(e) as being anticipated by Abe et al (US Patent no 6,674,623 B1).

4. As per claim 1, Abe et al teach

detecting that a processor is overheated [fig. 41; col. 29, lines 58-60; built-in temperature sensor to detect overheating];

asserting a thermal trip signal from the processor [Fig. 41; a signal from the microcomputer through inverter 114 to disconnect the power source];

causing the processor to enter a halt state [Fig. 41; microcomputer enters a temporary halt state; col. 3, lines 11-21]; and

automatically removing power from the processor [fig. 41; col. 29, line 58 – col. 30, line 3; transistor switch 116 will be turned off automatically upon receiving the thermal trip signal from the microcomputer and thus automatically removing power from the microcomputer].

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

6. Claims 2, 9-10, 13-14 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Abe et al (US Patent no 6,674,623 B1) in view of Hollowell et al (US Patent no 5,590,061¹).

¹ Reference was cited in the prior office action (dated 12/12/03).

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7. As per claim 2, Abe et al disclose the invention substantially. Abe et al do not expressly disclose about rebooting the system. However, Hollowell et al clearly disclose about rebooting a computer system when the computer system is beyond the maximum rated temperature [col. 7, lines 15-23]. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the cited references as both are directed to the problem of overheating in a computer system. Moreover, by rebooting the computer system, the other components in the computer system besides the processor will be substantially saved from getting overheated.

8. As per claim 9, Abe et al disclose the invention substantially. Abe et al do not expressly disclose about assertion of a stop clock signal periodically. However, Hollowell et al teach that the processor interface periodically asserts a stop clock signal to the processor in response to a system reboot following the assertion of the thermal trip signal [col. 11, lines 47-49; repeated ON/OFF]. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the cited references as both are directed to the problem of overheating in a computer system.

9. As per claim 10, Hollowell et al teach that a status bit that is set in response to the assertion of the thermal trip signal, the status bit to indicate that the system reboot is in response to the assertion of the thermal trip signal [inherent to the system].

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10. As per claim 13, Hollowell et al teach reset logic to cause a system reset in response to the assertion of the thermal trip signal [col. 7, lines 15-23].

11. As per claim 14, Hollowell et al teach that the reset logic to cause the system reset in response to the assertion of the thermal trip signal after a predetermined period of the time had elapsed following the assertion of the thermal trip signal [time to save the state of the processor; col. 11, lines 9-12].

12. As per claim 16, Hollowell et al teach that the power management device to periodically assert a stop clock signal to the processor during and following the system reset [col. 11, lines 47-554].

13. Claims 3-7 and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Abe et al (US Patent no 6,674,623 B1), Hollowell et al (US Patent no 5,590,061¹) and further in view of Mittal et al (US Patent no 5,719,800¹).

14. As per claims 3 and 4, Abe et al and Hollowell et al disclose the invention substantially. Abe et al and Hollowell et al do not disclose expressly about throttling the processor and applying a reduced voltage to the processor following the reboot. However, a routineer in the art would know that it is obvious to do so upon rebooting the system as it does not require to run the processor at fast speed and so there is no need to apply full voltage as clearly disclosed by Mittal

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et al [col. 9, line 65 – col. 10, line 8]. Therefore, it would have been obvious to one of ordinary skill in the art to combine the cited references as these deal with power consumption and turning off the system or rebooting the system. Moreover, Mittal et al clearly shows how one can control the clock and voltage applied to a processor during rebooting process.

15. As per claim 5, Abe et al disclose the invention substantially. Abe et al do not expressly disclose about rebooting the computer system includes rebooting the computer system after a predetermined period of time following the detection of the overheated condition. However, Hollowell et al disclose that the system does not immediately reboot upon detection of overheat condition, but the rebooting is delayed for a time to save the state of the processor [time to save the state of the processor; col. 11, lines 9-12]. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the cited references as both are directed to the problem of overheating in a computer system. Moreover, before rebooting the computer system, it is important to save the state of the processor and thus there is need to delay the rebooting the system for a predetermined period of time following the detection of the overheated condition.

16. As per claims 6 and 15, Abe et al and Hollowell et al disclose the invention substantially. Abe et al and Hollowell et al do not disclose about rebooting the computer after the processor has cooled to a predetermined temperature. However, Hollowell et al provide enough time to cool down the processor below the threshold before it reboot the system as to save the state of the processor while it is off [col. 11, lines 9-15]. Therefore, it would have been obvious to one

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of ordinary skill in the art to provide a predetermined time before rebooting the system so that the processor can be cooled to a predetermined temperature.

17. As per claim 7, Hollowell et al teach detecting for a second time that the processor is overheated [col. 11, lines 47-53; system once more determines that internal system temperature is greater than or equal to the threshold temperature]; automatically removing power from the processor for a second time [col. 11, lines 47-53; power off signal to turn off processor]; and again rebooting the computer system [col. 7, lines 15-23; turning off the power to the whole computer system].

18. Claims 8 and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Abe et al (US Patent no 6,674,623 B1).

19. As per claim 8, Abe et al teach

a processor interface unit to monitor a thermal trip signal from a processor [fig. 41; element 114 monitors a thermal trip signal from the microcomputer]; and

a voltage regulator module interface to assert a power off signal to a voltage regulator module in response to an assertion of the thermal trip signal [fig. 41; element 114 asserts a power off signal to element 116 to cut off the power].

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Abe et al do not expressly disclose about having a voltage regulator module interface to assert a power off signal to a voltage regulator module. But, transistor switch (element 116) acts as a voltage regulator switch that is used to control the power supply on/off to the microcomputer. However, a routineer in the art would easily be able to replace the element 116 with a voltage regulator module as a voltage regulator module is well known in the art. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to substitute the transistor switch (element 116) with a voltage regulator module interface as a voltage regulator module will also provide a variable control of power supply to the microcomputer besides just power on/off.

20. As per claim 11, Abe et al teach that

a processor including a thermal trip signal that is asserted in response to an overheat condition [fig. 41; col. 29, lines 58-60; built-in temperature sensor to detect overheating];

a power management device to receive the thermal trip signal, the power management device to assert off signal in response to an assertion of the thermal trip signal [fig. 41; element 114 monitors a thermal trip signal from the microcomputer]; and

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a power supply device to deliver power to the processor, the power supply device to receive the power off signal and to cease to deliver power to the processor in response to an assertion of the power off signal [fig. 41; element 114 asserts a power off signal to element 116 to cut off the power].

Abe et al do not expressly disclose about having a power management device. But, element 114 acts as a power management power device as it receives the thermal trip signal and sends a power off signal to cease to deliver power to the microcomputer thereon. However, a routineer in the art would be able to substitute the element 114 with a power management device, as a power management device is well known in the art. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to add a power management device with or in place of the element 114 as a power management will also provide a different mode of operations besides just power on/off.

21. As per claim 12, Abe et al disclose the invention substantially. Abe et al do not disclose that the power supply device is a voltage regulator module. However, a routineer in the art would know that usually a power supply device is a voltage regulator, as it is well known in the art to use a voltage regulator to regulate the supply of the power to a processor accordingly. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have a voltage regulator as a power supply device. Moreover, a voltage regulator will provide a variable power supply as needed besides just power on/off.

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Conclusion

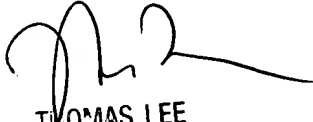
Any inquiry concerning this communication or earlier communications from the examiner should be directed to Suresh K Suryawanshi whose telephone number is 703-305-3990 (starting 10/18/04, please use 571-272-3668). The examiner can normally be reached on 9:00am - 5:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Thomas C. Lee can be reached on 703-305-9717 (starting 10/18/04, please use 571-272-3667). The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

sks

September 7, 2004


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